AMENDMENTS TO THE CLAIMS

1-14. (Cancelled)

15. (Currently Amended) A CMP rework method, comprising the steps of:

providing a semiconductor substrate which has a patterned dielectric layer, a barrier layer over the patterned dielectric layer, and a conductive layer over the barrier layer;

performing a first CMP process to remove part of the conductive layer;

depositing a layer of material ~~with a planar surface~~ substantially the same as the conductive layer over the conductive layer, wherein an entire upper surface of the layer of material is planar; and

performing a second CMP process to expose the patterned dielectric layer.

16. (Original) The method as claimed in claim 15, wherein the conductive layer comprises copper or copper alloy

17. (Original) The method as claimed in claim 15, wherein the dielectric layer comprises silicon dioxide, silicon nitride, phosphosilicate glass, borophosphosilicate glass, or fluorosilicate glass

18. (Original) The method as claimed in claim 15, wherein the barrier layer comprises Ta, Ti, TaN, TiN, or WN.

19. (Original) The method as claimed in claim 16, wherein the deposition of copper or copper alloy is performed using electroplating, CVD, or PVD.

20. (Previously Presented) The method as claimed in claim 15, wherein the top surface of the layer deposited in said step of depositing said layer of material substantially the same as the conductive layer over the conductive layer is higher than the barrier layer.

21. (Previously Presented) The method as claimed in claim 15, wherein the semiconductor substrate is reported by a CMP machine as an abnormally polished wafer at a predetermined CMP end point after performing said first CMP process to remove part of the conductive layer.